REMARKS

In response to the Office Action mailed August 5, 2004, Applicant amends his application and requests reconsideration. In this Amendment claims 2 and 9 are cancelled and claim 14 is added so that claims 1, 3-8, and 10-14 are now pending.

There is an error in the PTO-892 form supplied with the Official Action. As informally discussed with the Examiner, the patent number of the second listed reference is incorrect and should be U.S. Patent 6,675,319 to Chen. The correction was supplied informally in order to permit preparation of a response to the Office Action. Appropriate correction of the record of this patent application is respectfully requested.

Claims 4-7 and 9-13 were indicated to be allowable, if rewritten in independent form. In this Amendment claim 4 is rewritten in independent form so that claims 4, 5, and 7, should be immediately allowed. Although claim 6 was indicated to be allowable, that claim has not been rewritten in independent form. Claim 9 inadvertently depended from claim 5 but should have depended from claim 8. This amended claim 9 has been rewritten in independent form as amended claim 8. It is believed the indicated allowability of claim 9 still applies with respect to the correct dependency of that claim. In addition, claim 11 has been rewritten in independent form. Therefore, claims 8 and 10-14 should be immediately allowed.

In rewriting claims in independent form, amendments have been made to produce compact claims, to eliminate inconsistencies between the language of the examined claims, and to account for claim cancellations so that no claim depends from a cancelled claim. However, there has been no substantive change of any of these claims.

In this Amendment claim 2 is also rewritten in independent form as amended claim 1. Therefore, the only prior art rejections that require response are the rejections of examined claims 2 and 3. Claim 2 was rejected as unpatentable over Jeddeloh (U.S. Patent 5,862,314 in view of Brauch et al. (U.S. Patent 6,550,023, hereinafter Brauch). Claim 3 was rejected over the same combination of references and further in view of Kaiser et al. (U.S. Patent 6,728,902, hereinafter Kaiser). These rejections are respectfully traversed.

The invention as defined by amended claim 1 concerns a semiconductor device including two separate chips. The first chip includes an electrically rewritable nonvolatile memory. The second chip includes a memory with a redundant circuit and a circuit for a memory test that includes a nonvolatile memory. That nonvolatile memory of the second chip stores a test program, a repair analysis program, and a software repair program. As described in the patent application, the invention provides several advantages. First, by

employing separate chips, manufacturing cost can be reduced because chips with different kinds of memories can be separately manufactured. The process of manufacture is simplified by restricting the type of memory on a particular chip. Second, the invention provides a software repair for a defective memory area and not the kind of hardware repair that employs fuses. Thus, the repair can be dynamic and adapt to a particular fault situation. In addition, there is no danger of damage to any of the chips that can occur when energy is supplied for opening a fuse.

The rejection is erroneous because there is no suggestion for modifying the principal reference, Jeddeloh, with the cited disclosure of Brauch. In applying Jeddeloh in rejecting examined claim 1, the Examiner relied upon Figure 1 of Jeddeloh and the description regarding the memory module 12 that appears in columns 2 and 3 of Jeddeloh. Jeddeloh's memory module 12 includes a nonvolatile memory block 16 and a volatile memory block 14. These two kinds of memory blocks are never suggested or described as being on different chips. In making the rejection, it has obviously been assumed that these two memory blocks of Jeddeloh are actually different memory chips. Assuming, for the sake of argument, that the two blocks 14 and 16 represent different chips, then no suggestion can be found in Brauch for modifying what is described by Jeddeloh to produce the invention as defined by amended claim 1.

Brauch describes a single chip integrated circuit 2 that includes a memory 4, a built-in self test functional block 6, and a communication port 8, among other elements. The Examiner asserts that the built-in self test functional block 6 includes a nonvolatile memory. This assertion is apparently based on an implication that the test circuit must include in memory a test program rather than on the express disclosure of Brauch. Thus, Brauch does not seem to support the Examiner's position. However, even if the Examiner's position is accepted for the sake of argument, not only with regard to Brauch but with respect to Jeddeloh in the rejection of examined claim 1, then it becomes apparent that the rejection of examined claim 2 is erroneous because it is founded upon one inference piled upon a second inference.

In rejecting claim 1, it is clear from the Office Action that the Examiner assumed that the memory blocks 14 and 16 of Jeddeloh are separate memory chips even though there is no express description in Jeddeloh that such a situation exists. The Examiner's position might be supported based upon the different manufacturing processes for the two different kinds of memories, simplifying the manufacturing of the two different memories on separate chips. Given that assumption, it would not be reasonable to assert that Brauch would suggest a modification of Jeddeloh by including in the volatile memory

block 14 the functional block 6 of Brauch, which includes a nonvolatile memory, the volatile memory 4 of Brauch. The same reasoning applies, in reverse, with respect to the nonvolatile memory block 16 of Jeddeloh. A person dividing these two kinds of memories into different chips would not modify a nonvolatile memory chip by including both volatile and nonvolatile memories in that chip as in the integrated circuit 2 of Brauch. Thus, the rejection of claim 2, now appearing as claim 1, is erroneous if the rejection of examined claim 1 is accepted. If the Examiner disagrees with this analysis, then he should indicate that the original rejection of claim 1 is withdrawn because Jeddeloh does not clearly describe separate first and second chips having the memories described in examined claim 1.

Since the foregoing remarks demonstrate that amended claim 1 is clearly patentable over the asserted combination of Jeddeloh and Brauch, claim 1 should be allowed. It follows that claim 3, even if its limitation is described by Kaiser, must also be allowed since that claim 3 depends from amended claim 1.

Reconsideration and allowance of all claims now pending are earnestly solicited

Respectfully submitted,

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